



The domino sampling chip: a 1.2 GHz waveform sampling CMOS chip

Christian Brönnimann^{a,*}, Roland Horisberger^b, Roger Schnyder^b

^aSwiss Light Source, Paul Scherrer Institut PSI, 5232 Villigen-PSI, Switzerland

^bPaul Scherrer Institut PSI, 5232 Villigen-PSI, Switzerland

Received 5 June 1998

Abstract

A waveform digitizing system is developed at the Paul Scherrer Institute (PSI) based on the Domino Sampling Chip (DSC), a fast analog memory fabricated in CMOS technology. The principle of operation, the test system and the performance of the chip are described. Sampling frequencies of 1.2 GHz are generated on chip; the analog waveform is stored in 128 sampling capacitors. The main parameters of the chip are: timing non-linearity of 0.08%, amplitude non-linearity of 0.2% and a read-out frequency of 2.5 MHz. The design of the chip is optimized for a multi-channel board with parallel sampling of 16 input channels upon a common trigger pulse. © 1999 Elsevier Science B.V. All rights reserved.

1. Introduction

A number of waveform digitizing systems have been developed for High Energy Physics (HEP) systems in which detector signals are captured as “snap shots”, i.e. sampled at a high frequency for a limited period of time. The samples are e.g. stored in a fast analog memory and retrieved at a lower rate, i.e. digitized with a commercial ADC before a new waveform is acquired. This technique was successfully realized in switched capacitor circuits [1–4]. Applications based on such samplers usually consist of hundreds of analog channels which need

to be sampled, therefore requiring low cost devices [4,5]. Other waveform digitizing systems are based on GaAs CCDs, which are used for particle identification and pile-up rejection in large HEP detectors [6,7].

For a precise determination of the pion beta decay rate $\pi^+ \rightarrow \pi^0 e^+ \nu_e$ ($BR \sim 10^{-8}$) a new detector is currently being built at the Paul Scherrer Institute (PSI) [8–10]. In order to obtain the required statistics, the experiment is performed at beam stopping rates of $5 \times 10^6 \pi^+ / s$. The essential part of the detector is a spherical calorimeter consisting of 240 pure CsI crystals, which emit light with a decay time of 20 ns. In spite of the fast decay time, one has to deal with an increased probability of background from pile-up pulses, which can be evaluated by sampling and digitizing the individual crystal signals.

*Corresponding author. Tel.: + 41 56 310 37 64; fax: + 41 56 310 31 51; e-mail: broennimann@psi.ch

In order to reduce the costs for the entire waveform digitizing system, the waveforms stored in the samplers are read-out serially and are multiplexed into one ADC channel. This on the other hand rises the read-out dead-time per event introduced in the detector system, which can usually not be tolerated. Thus, zero suppression is of high importance for the successful implementation of a waveform digitizing system.

This work presents the performance of a dedicated CMOS chip for use with fast analog signals from an amplifier (e.g., a photomultiplier tube) with signal amplitudes of several hundred mV. The storage depth of the chip is about 100 ns. It is the final version of several CMOS circuits designed at PSI [10–13]. The main advantage of the DSC over commercially available flash ADCs is its inherent high sampling speed of 1.2 GHz, the low power dissipation and the very low cost per chip. The chip is optimized to be used in a large waveform digitizing system, each chip has a zero suppression circuit.

2. System description

2.1. Operation of the DSC

The chip is realized in the S1DM (1 μm SACMOS double metal) process offered by Philips

Semiconductors AG, Switzerland. The operation of the DSC consists of a sampling phase and a readout phase. The principle of the sampling mechanism is based on the transmission of a logic pulse through two sequential CMOS inverters. The average gate delay time for a minimum sized transistor is ~ 400 ps in the present design, resulting in a delay of approximately 800 ps per inverter pair. Thus a logical signal propagating through a long chain of inverters acts like a domino wave (thus the name domino sampling chip).

The circuit diagram of the DSC is shown in Fig. 1. A positive edge applied at the GATE pad starts the domino wave which after every second inverter connects the read-in line over the switches S1–S128 to the sampling capacitors C1–C128 (0.2 pF). The charge stored on the capacitors is proportional to the momentary voltage level on the input bus. Four additional cells A1–A4 are provided which sample the externally supplied voltage V_{ADDR} used for an analog chip identification when read-out in zero suppression mode (see below). A discharge switch has been implemented for each cell, which keeps all the sampling capacitors at the same potential. It prevents the capacitors from charging up before a waveform is acquired. The switch is opened by the GATE pulse and closed with the RBO pulse, i.e. after the read-out of the chip.

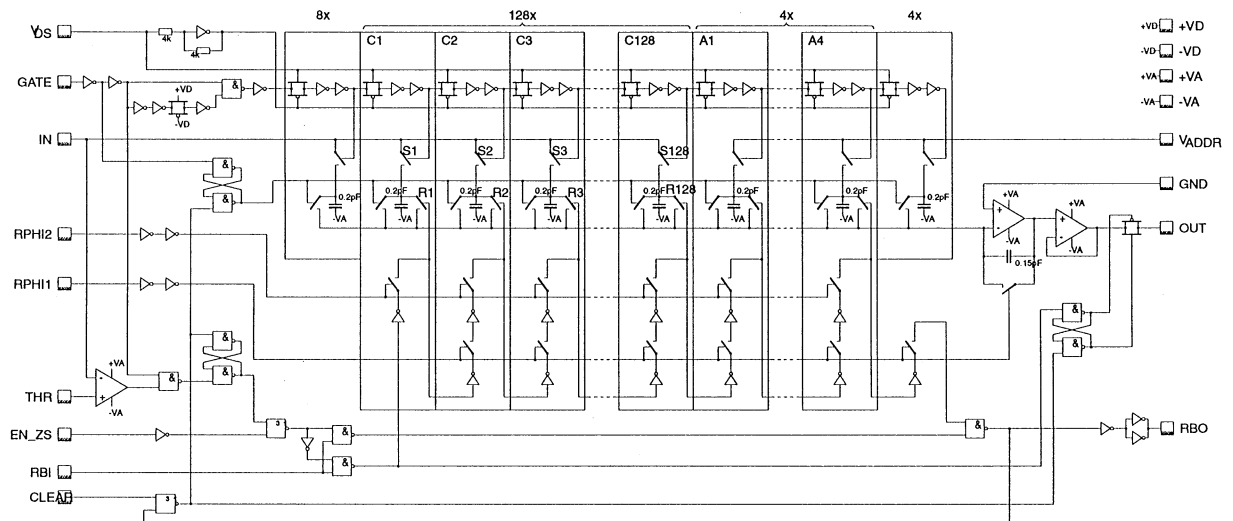


Fig. 1. Simplified circuit diagram of the Domino Sampling Chip.

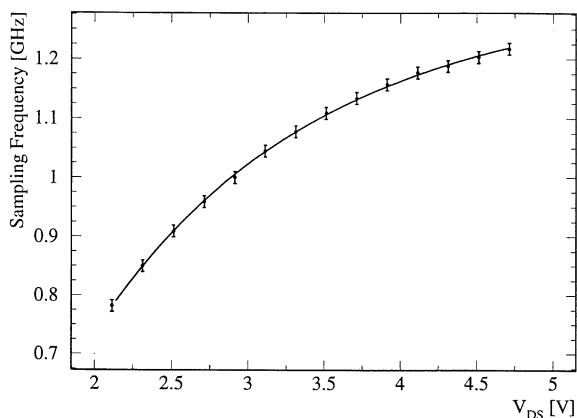


Fig. 2. Sampling frequency as a function of the control voltage V_{DS} . The solid line is fit to the data with the theoretical delay for 2 inverters and a NMOS transistor.

The speed of the sampling mechanism is controlled by the domino speed voltage v_{DS} , which influences the propagation time of the domino wave. For values of $2\text{ V} < v_{DS} < 4.7\text{ V}$ sampling frequencies between 0.8 and 1.2 GHz are obtained (Fig. 2).

The input signal is DC-coupled to the DSC IN pad, the input capacitance is approximately 1 pF. Thus, no internal bandwidth restriction other than the Nyquist limit is present, i.e. the maximum detectable frequency in the spectrum of the analog signal is half the sampling frequency.

The read out of the stored information is done using a standard 2-phase shift register: The RBI (read bit in) pulse is clocked through the read-out shift register with the non-overlapping signals $R\phi_1$ and $R\phi_2$. Synchronous with the $R\phi_2$ -pulse the corresponding capacitor is connected over the read-out line to the charge-sensitive output amplifier, which is reset with the $R\phi_1$ -pulse. At the 132th clock cycle, the RBO (read bit out) pulse appears at the end of the shift register, indicating the successful read-out of the chip. This pulse disconnects the amplifier from the output pad, thus enabling the serial read-out of several DSCs connected to the same output line. The RBO -pulse can be used as a RBI for the next chip in the chain. The maximum read-out frequency is 5 MHz, which corresponds to a dead-time of 25.6 μs for one DSC.

The final read-out architecture for the pion beta decay experiment is based on multiplexing 16

DSCs to one single analog output line connected to one commercial ADC with an appropriate sized memory. A full read-out sequence of 16 DSCs corresponds to a dead-time of 0.8 ms, which is not tolerable. Thus a zero-suppression circuit has been implemented on each DSC, which prevents the chip from being read-out, when the analog signal is below the threshold or not in coincidence with the $GATE$ -pulse [10]. The zero suppression can be enabled or disabled.

2.2. Experimental setup

The experimental setup comprises a PC board, on which the DSC resides, NIM trigger electronics, CAMAC units (ADC, IO-unit, and PDG4222), an IBM compatible 486 personal computer and dedicated units to supply test waveforms. The PC board supplies the necessary analog voltages and the digital signals for the DSC operation. The logic signals provided to the DSC are TTL signals shifted to “0” = -1.5 V and “1” = 3.5 V , relative to the analog ground. The $GATE$ signal is the trigger for the domino wave and needs to arrive 20 ns before the analog signal. From an external 2.5 MHz sinusoid the read-out clock signals are generated on board upon arrival of the $START$ pulse. During the read-out phase, the analog signal line is still connected to the IN pad, but no distortion of the output due to further input signals has been observed.

The analog OUT of the chip and the $CONVERT$ signal (TTL signal, synchronous to ϕ_2) are supplied to a flash ADC which converts the analog data and stores the digitized information in its internal buffer. The CAMAC crate is controlled via a HYTEC 1331 Turbo CAMAC-PC interface. The gains of the amplifier on the PCB board and the SIROCCO III analog input card were chosen such that 1 ADC count corresponds to approximately 2 mV input voltage.

The electronics can be triggered by an external signal, which latches the event coincidence, and causes the DSC to sample the analog input. The analog to digital conversion of the “analog information” is begun 1 μs after the sampling and requires 51.2 μs . Now, a LAM signal is supplied to the CAMAC-IO and subsequently the CAMAC

ADC is read out. The system is controlled by a dedicated data-acquisition program written in C-language. It includes an online analyzer which displays the acquired waveform and a number of user defined histograms. The waveform data are stored to disk for further analysis.

3. Performance

Before each set of measurements a pedestal run was performed, with the DSC analog IN shorted to (analog) ground. Pedestals and noise of each bin were calculated as mean and rms values of 1000 events. The maximum pedestal variation is 2.5 ADC counts, i.e. 5 mV equivalent input voltage. The noise values are constant over all bins and are 1.3 ADC counts, i.e. 2.7 mV. This value includes the noise of the complete electronics chain including the PCB board and the ADC. Especially the on-board generation of the TTL CONVERT pulse for the ADC has been found to be a major source of disturbance.

3.1. Amplitude non-linearity

The amplitude non-linearity of the system was tested using DC voltages supplied by a Kethley Multimeter. DC-levels between -1 and $+1$ V were sampled with 1.2 GHz and read out with 2.5 MHz. For each level 500 events were recorded. Fig. 3 shows the mean output ADC-value of one bin as a function of the input DC-level. In the range of $[-300$ mV, $+400$ mV] the peak deviation from linearity is 0.8 ADC counts, which corresponds to an amplitude non-linearity of 0.2%. By appropriate choice of the DSC analog ground level, the range can be shifted to, e.g., $[-700$ mV, 0 mV] which is suitable for the PMT-signals in case of the pion beta decay experiment. The range is limited by the setting time of the on-chip output amplifier and can be increased by decreasing the read-out speed.

3.2. Timing non-linearity

With timing non-linearity we refer to the possible variation of the inverter gate delays that are responsible for the sampling speed. The timing non-

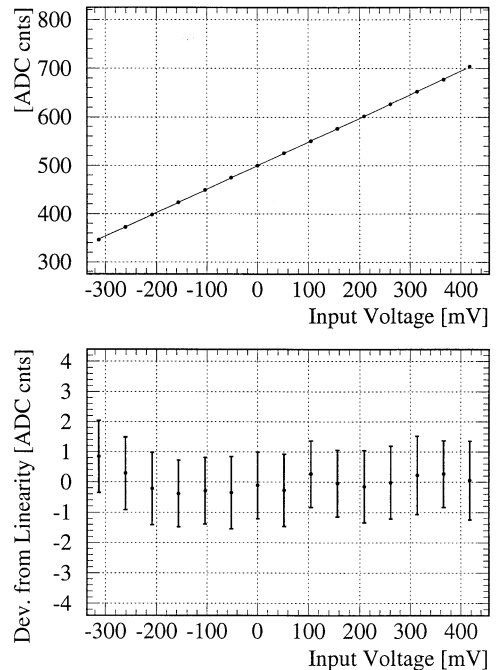


Fig. 3. (Top) Mean ADC values of 500 events of a single bin as a function of input voltage. (Bottom) Residuals from the fit, the error bars are the rms values.

linearity was determined by mapping out the transition levels between the DSC bins. The negative edge of a NIM signal with an amplitude of -800 mV and a rise time of 2 ns was applied to the chip and sampled with 1.2 GHz. With a simple algorithm, the bin at which the output signal crossed a threshold of -400 mV was determined in software and filled into a histogram. The delay of the input signal was chosen such that its edge fell between bin i and $i + 1$. In order to access all the bins on the DSC, a coarse delay relative to the GATE signal of 20–120 ns had to be established; furthermore the delay had to be varied in the range of ps in order to match the 50–50 transition point between two neighboring bins. The NIM pulse was generated by using a LeCroy 4222 CAMAC programmable gate and delay generator, which produces precise time delays up to 16.7 ms in 1 ns increments synchronously with a random trigger input. The fine delay was established using a coaxial delay tube, used for high frequency tuning, the length of which could be varied manually in mm steps be-

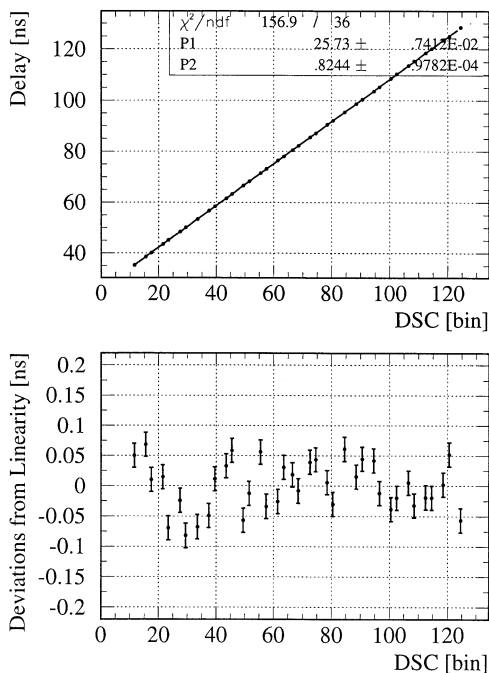


Fig. 4. Total delay (coarse + fine) to access transitions between bins. The solid line is a linear fit to the data (Top). Deviations from the linear fit (Bottom). The maximum deviation is 80 ps.

tween 0 and 22 cm. The delay of the device was 33.5 ± 0.5 ps/cm, leading to a maximum delay of 0.736 ns. The combination of coarse delay with the 4222 and the mechanical fine delay made it possible to reach almost all of the 127 transitions between bins. From these data the resulting non-linearity was calculated: As can be seen from Fig. 4, the maximum deviation from linearity is 80 ps over the 100 ns range, which corresponds to a timing non-linearity of 0.08% at 1.2 GHz sampling frequency. The timing non-linearity at a sampling speed of 1 GHz is well below 0.8% and rises to 1.3% at 0.2 GHz.

In Ref. [10], the timing resolution of the previous version of the DSC (700 MHz) was determined relative to a Philips Scientific 10C6 FASTBUS 10-bit TDC with a LSB¹ of 100 ps. With a simple linear interpolation algorithm, a resolution of

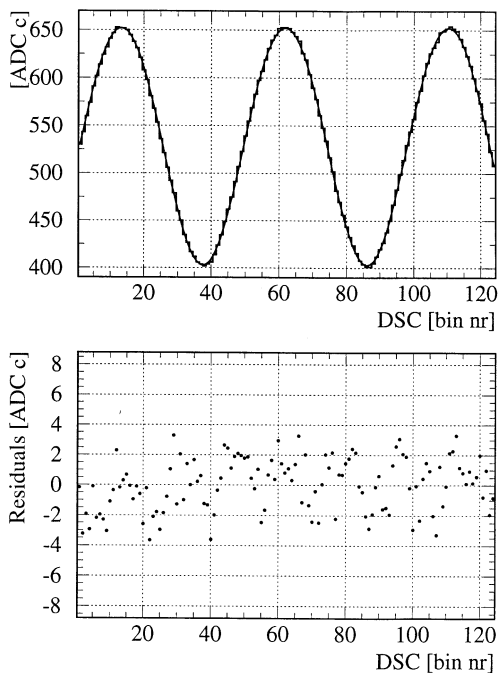


Fig. 5. (Top) The response to a 500 mVpp, 25 MHz sine wave sampled at 1.2 GHz together with the fit (solid line). (Bottom) The residuals of the fit.

200 ps (rms) was obtained. The increased sampling speed of the present chip should allow timing resolution of the order of 100 ps.

3.3. Tests with sine waves

The response of the DSC to sine waves was measured by using a WAVETEK 178 50 MHz waveform synthesizer. Reference measurements of 25 MHz sinusoidal signals with variable amplitudes of the synthesizer were performed with a TEKTRONIX TDS744 digital scope. The signals were sampled with 1 GHz/s and the digital data were analyzed offline. The sinusoidal waveforms were best fitted with the fundamental 25 MHz sine wave and a 2% additional 2nd harmonic sinusoid.

Free running sinewaves of different amplitudes and frequencies were applied to the DSC. A pedestal measurement was performed prior to the events with sine waves, and pedestals were subtracted from the data. Fig. 5 top panel shows the result of a 500 mV_{pp} amplitude, 25 MHz sine wave, plot-

¹ Least significant bit.

Table 1

DSC parameters and performance under experimental conditions for the given input range

Nr of Bins	128
Input range	± 0.35 V
Maximum sampling frequency	1.2 GHz
Read out frequency	2.5 MHz
Noise (rms)	2.6 mV
Pedestal variation (max)	± 2.5 mV
Timing non-linearity (for 100 ns range)	0.08%
Amplitude non-linearity (700 mV range)	0.2%

ted together with a fit function of the above stated form. The rms-value of the residuals from the fit, shown in Fig. 5 bottom panel, is 3 mV. The response of the DSC to the sinusoidal signals is identical to that of the digital scope.

4. Conclusions and outlook

This work presents the performance of the Domino Sampling Chip (DSC), a CMOS analog sampling circuit which is being developed for the pion beta experiment at PSI. A test system was set up in order to measure the chip performance. A summary of the important parameters is shown in Table 1.

The circuit of the DSC is designed such that a large number of chips (planned are 128) can be

integrated on one NIM-board, which leads to very low costs per digitizing channel. Due to the integrated zero suppression circuit, the (analog) outputs can be multiplexed onto one ADC with acceptable dead time. All in all this allows to build a large, high speed, waveform digitizing system with the presented performance for costs below 100 SFr per digitizing channel.

References

- [1] S. Kleinfelder, IEEE-Trans. Nucl. Sci. 35 (1988) 151.
- [2] S. Kleinfelder, IEEE-Trans. Nucl. Sci. 37 (1990) 1230.
- [3] G.M. Haller, B.A. Wooley, IEEE J. Solid State Circuits 29 (4) (1994) 500.
- [4] G.M. Haller, B.A. Wooley, IEEE Trans. Nucl. Sci. 41 (4) (1994) 1203.
- [5] S.R. Klein et al., IEEE Trans. Nucl. Sci. 43 (3) pt. 2 (1996) 1768.
- [6] M. Atiya et al., Nucl. Instr. Meth. A 279 (1990) 180.
- [7] D. Bryman et al., IEEE Trans. Nucl. Sci. 38 (2) (1991) 295.
- [8] D. Pocanic, A precise measurement of the $\pi^+ \rightarrow \pi^0 e^+ \nu_e$ decay rate, PSI Proposal R-89-01, 1989.
- [9] K.A. Assamagan, Ph.D. Thesis, University of Virginia, 1995.
- [10] Ch. Brönnimann, Ph.D. Thesis, University of Zürich, 1996.
- [11] Monika Brogle, Testing a CMOS Waveform Sampling Chip, PSI Internal Report, TM-11-90-02, 1990.
- [12] Ch. Brönnimann, R. Horisberger, Testing the Domino Sampling Chip, PSI Internal Report, TM 11-94-02, 1994.
- [13] D. Goldner et al., Study of time and charge resolution of drift chamber pulses using a fast VLSI waveform sampler chip, PSI-PR-95-10, June 1995.